an ESD negative line; and

a plurality of floating lateral clamp diodes connected to the pad so that a first floating lateral clamp diode is connected to the pad and the positive line, and a second floating lateral clamp diode is connected to the pad and the negative line, a floating lateral clamp diode of the plurality of floating lateral clamp diodes having:

a well of a second conductivity type formed in the substrate, the well having a top surface and a dopant concentration;

a plurality of spaced-apart first regions of the first conductivity type formed in the well, each first region having a top surface, the plurality of first regions being electrically connected together, and formed in the well so that the top surface of the well encircles the top surface of each first region; and

a second region of the second conductivity type formed in the well, the second region having a top surface, and being formed so that the top surface of the second region encircles the top surface of the well that encircles the top surface of each first region, the second region having a dopant concentration that is greater than the dopant concentration of the well.

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10. (Amended) [The chip of claim 1 wherein] A semiconductor chip having a substrate of a first conductivity type, the chip comprising:

a pad;

an electrostatic discharge (ESD) positive line, the ESD positive line not being connected to a voltage source;

an ESD negative line; and

a plurality of floating lateral clamp diodes connected to the pad so that a first floating lateral clamp diode is connected to the pad and the positive line, and a second floating lateral clamp diode is connected to the pad and the negative line, a floating lateral clamp diode [comprises] having:

a well of a second conductivity type formed in the substrate, the well having a surface and a dopant concentration; and

a first region of the second conductivity type formed in the well, the first region having a surface, and a dopant concentration that is less than the dopant concentration of the well;

a plurality of spaced-apart second regions of the first conductivity type, each second region having a surface, the plurality of second regions being electrically connected together, and formed in the first region so that the surface of the first region encircles the surface of each second region.

11. (Amended) The chip of claim 10 and further comprising a third region of the second conductivity type, the third region having a top surface, and being formed in the first region so that the top surface of the third region encircles the top surface of the first region that encircles the top surface of each second region, the third region having a dopant concentration that is greater than the dopant concentration of the well.

15. (Amended) A semiconductor chip having a substrate of a first conductivity type, the chip comprising:

a plurality of pads;

an electrostatic discharge (ESD) negative ring;

a plurality of ESD positive lines, the plurality of positive lines not being connected to a steady voltage source;

a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each positive line is connected to the negative ring via an ESD switch;

a plurality of first floating lateral clamp diodes connected to the pads so that each first floating lateral clamp diode is connected to a pad and the negative ring; and

a plurality of second floating lateral clamp diodes connected to the pads so that each second floating lateral clamp diode is connected to a pad and a positive line.

18. (Amended) The chip of claim 17 and further comprising a second region of the second conductivity type formed in the well, the second region having a top surface, and being formed [in the well] so that the top surface of the second region encircles the top surface of the well that encircles the top surface of each first region, the second region having a dopant concentration that is greater than the dopant concentration of the well.

21. (Amended) The chip of claim 20 and further comprising a third region of the second conductivity type, the third region having a top surface, and being formed in the first region so that the top surface of the third region encircles the top surface of the first region that encircles the top surface of each second region, the third region having a dopant concentration that is greater than the dopant concentration of the well.

Please add the following new claims:

--32. The chip of claim 1 wherein the chip has a periphery, and the ESD positive line extends around the periphery of the chip.

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33. The chip of claim 1 and further including a number of ESD switches connected to the ESD positive line and the ESD negative line.

34. The chip of claim 32 wherein the ESD switches are located between two adjacent corners of the chip.

35. The chip of claim 34 wherein an ESD switch is positioned adjacent to one of the two adjacent corners.

36. The chip of claim 1 and further comprising:

a steady voltage line unconnected to the ESD positive line; and

a driver transistor connected to the steady voltage line and the pad.--

REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is requested. Claims 1, 5, 6, 10-11, 17-23, and 32-36 are now in this application. Claims 1, 10, 11, 15, and 18 have been amended. Claims 2-4, 7-9, 16, and 24-31 have been cancelled. (Claims 12-14 were previously cancelled.) Claims 32-36 have been added.